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Experimental Validation of a Three-Phase Voltage-Source Inverter with SPWM Modulation for Low-Voltage Microgrid-Oriented Applications

Validación experimental de un inversor trifásico de fuente de voltaje con modulación SPWM para aplicaciones de baja tensión orientadas a microrredes

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ABSTRACT

This work presents the design, implementation, and experimental validation of an open-loop three-phase inverter prototype. The experimental campaign was carried out with a regulated 48 V DC bus, while the bus-monitoring circuit was dimensioned for a wider voltage range. Control was implemented on an STM32 using digital SPWM, with a 120° phase shift and an adjustable output frequency between 60 and 80 Hz. To reduce the risk of cross-conduction in the MOSFETs, dead-time insertion was configured in both hardware and firmware. Tests with resistive loads verified three-phase operation in star and delta configurations, with balanced line voltages under laboratory conditions. The efficiency close to 92% corresponds to the tested low-load condition. Characterization at higher power levels and harmonic-distortion measurements are proposed as the next validation stage.

Keywords: Dead-time, Energy Efficiency, MOSFET, SPWM Modulation, Three-phase Inverter.

RESUMEN

Este trabajo presenta el diseño, la implementación y la validación experimental de un prototipo de inversor trifásico en lazo abierto. La campaña experimental se realizó con un bus DC regulado de 48 V, mientras que el circuito de monitoreo del bus fue dimensionado para un rango mayor de tensión. El control se implementó en un STM32 mediante modulación SPWM digital, con desfase de 120° y frecuencia de salida ajustable entre 60 y 80 Hz. Para reducir el riesgo de conducción cruzada en los MOSFETs, se configuró inserción de tiempos muertos en hardware y firmware. Las pruebas con cargas resistivas permitieron verificar la operación trifásica en configuraciones estrella y delta, con tensiones de línea balanceadas bajo las condiciones de laboratorio. La eficiencia cercana al 92% corresponde a la condición de baja carga ensayada. La caracterización a mayor potencia y la medición de distorsión armónica se plantean como la siguiente etapa de validación.

Palabras Clave: Dead-time, Eficiencia Energética, MOSFET, Modulación SPWM, Inversor Trifásico.

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I. Introducción

The conversion of direct current (DC) energy into three-phase alternating current (AC) is a fundamental process in power electronics [1], particularly for supplying loads from low-voltage 48 V DC buses [2]. During this conversion process, one of the most critical challenges in bridge inverter topologies is preventing cross-conduction between switching devices. To avoid this short circuit, it is essential to design algorithms that inject precise dead-times, considering that an incorrect configuration can severely distort the output voltage [3].

Due to its ease of implementation, SPWM modulation remains one of the main methods for controlling three-phase inverters and transforming switching signals into alternating voltage using six transistors. As demonstrated by previous work on MOSFET-based inverters coupled to star-connected loads, the key to obtaining an optimal output voltage lies in the precise design of the switching patterns and maintaining grid balance [4].

Recent works have shown the relevance of studying the behavior of inverters under real operating conditions and the possible degradation of power devices. In [5], the effect of variations in the on-state resistance of MOSFETs on phase imbalance, total harmonic distortion, and the stability of a three-phase inverter is analyzed, using a validation strategy based on MIL, SIL, and PIL on an STM32 platform. Likewise, [6] presents a hybrid DC/AC conversion topology with modified SPWM modulation, inherent protection against shoot-through, and experimental validation in a low-power prototype.

In this context, the present work focuses on the design, implementation, and laboratory validation of an open-loop SPWM three-phase inverter, with dead-time insertion and tests on balanced resistive loads in star and delta configurations.

The development of the three-phase inverter was structured based on an analytical and modular design, dividing the system into control, power, and validation stages. The prototype was dimensioned to operate at low voltage. The experimental validation was carried out using a regulated DC bus close to 48 V, while the bus measurement circuit was designed with sufficient margin for nominal and overvoltage conditions. Based on these specifications, the load capacity and the protection elements against thermal and voltage transients were dimensioned.

II. Metodología

Table I. Design parameters and test conditions

Parameter	*Symbol*	*Value used*
Bus DC de ensayo	*(V_{DC})*	*48.87 V*
DC bus sensing range	—	*0–50 V DC*
PWM switching frequency	*(f_s)*	*3 kHz*
Dead-time	*(t_d)*	*1.5 (μs)*
Output frequency	*(f_o)*	*60-80 Hz*
Modulation technique	—	*SPWM*
Power devices	—	*6 MOSFETs IRFP460A*
Gate drivers	—	*IR2010*
Load type	—	*Resistive*
Nominal load resistance	*(R_L)*	*(≈620 Ω)*
Load connection	—	*Star / Delta*
Measured current per branch	*(I_r)*	*33.65 mA*
Input power	*(P_{in})*	*6.793 W*
Calculated output power	*(P_{out})*	*6.3156 W*
Experimental efficiency	*(η)*	*92.97 %*

To summarize the design parameters and the conditions used during the experimental tests, Table I presents the main operating variables of the three-phase inverter. These values include the DC bus, the switching frequency, the dead-time, the load configuration, and the electrical quantities recorded for the power and efficiency calculations.

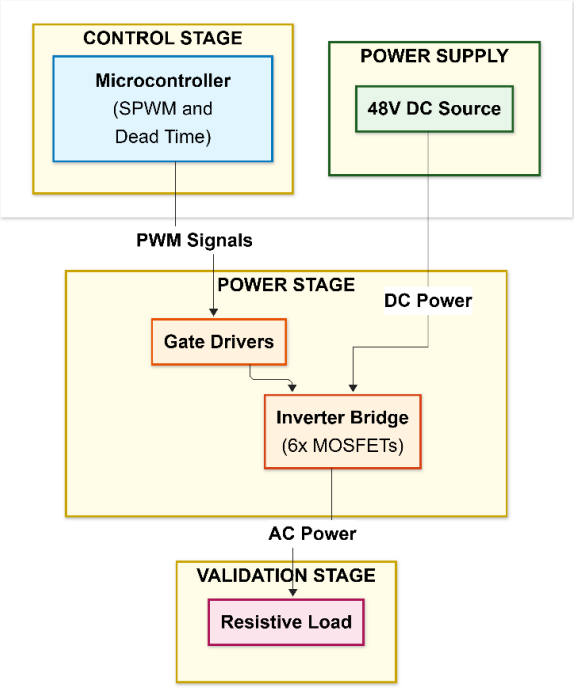


Fig. 1: *Block diagram of the three-phase inverter architecture and power flow.*

A. General System Architecture

The converter topology is based on a three-leg inverter bridge architecture. Fig. 1 illustrates the general block diagram of the implemented system. For energy conversion, a classical inverter bridge topology was implemented. The component-level design is detailed in Fig. 2, which shows the electrical schematic with the half-bridge configuration for each of the three phases.

The system is powered by a stabilized DC power supply. The control stage calculates the switching patterns and sends PWM logic signals to the power stage. These signals are received by IR2010 gate drivers, which act as high-side/low-side drivers to condition the firing levels required by the six MOSFETs in the inverter bridge. Finally, the energy converted into three-phase alternating current is applied to the resistive load bank used for validation.

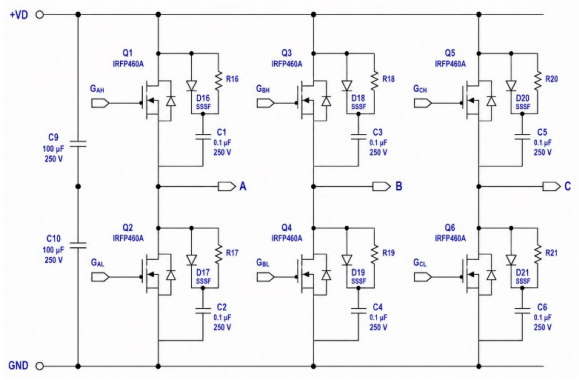


Fig. 2: *Electrical schematic of the power stage of the three-phase inverter.*

B. Firmware Development and Programming Environment

For the synthesis of Sinusoidal Pulse Width Modulation (SPWM) and the rigorous injection of dead times, the digital control was centralized in a 32-bit STM32 microcontroller with an ARM Cortex-M4 core (NUCLEO-F401RE board) [7].

Firmware programming, compilation and debugging was done in STM32CubeIDE. The generation of the SPWM signals was implemented using the advanced TIM1 timer, configured to operate with a switching frequency of 3 kHz and complementary outputs, avoiding software delays. The use of complementary channels allows the 1.5 µs dead-time timing to be concentrated on the microcontroller peripheral and reduces dependence on the firmware execution time [7], [8].

In addition, due to the digital nature of the modulation programmed in the STM32, the fundamental output frequency (f_m) is not limited to 60 Hz. The system allows this frequency to be dynamically adjusted simply by modifying the timer parameters in the firmware. This flexibility gives the prototype the ability to adapt to 50 Hz grids or to operate in variable-speed motor applications, without requiring any modification to the power hardware.

C. Nominal Power Capacity

To define the operating range of the system, the energy transfer capacity was analyzed, assuming an expected line-to-neutral RMS voltage of 120 V_{rms} per phase and a continuous load current I_L=5 A. Under these boundary conditions, the apparent power (S) supported by each phase of the inverter is determined by (1):

$$S = 120V \times 5A = 600\,VA \qquad (1)$$

For real application scenarios involving inductive loads, a standard power factor of 0.8 is assumed. Consequently, the nominal active power (P) delivered by the power stage is calculated using (2):

$$P = 600\,VA \times 0.8 = 480W \qquad (2)$$

These values define the thermal and conduction safety limits considered for selecting the semiconductor devices.

D. Design of the Snubber RCD Network

The parasitic inductances of the printed circuit board and wiring induce severe transient overvoltages (dv/dt) during the fast turn-off periods of the transistors. To absorb the reactive energy and limit voltage peaks, an RCD snubber network was designed and implemented in parallel with each semiconductor device [9].

The analytical dimensioning was carried out by extracting the dynamic parameters from the IRFP460A MOSFET datasheet [10] A fall time of t_f = 39 ns and a maximum continuous current of I_M=20 A at 25 °C, were considered, operating under a drain voltage of V_D= 170V and the nominal load current of I_L= 5 A.

The minimum value of the snubber capacitance (C_s) must guarantee a safe voltage level until the device current decreases to zero, and is calculated using (3):

$$C_s \geq \frac{I_L t_f}{2 \cdot V_D} = \frac{5\,A \cdot 3.9 \cdot 10^{-9} s}{2 \cdot 170\,V} \geq 0.573\,\eta F \qquad (3)$$

The network resistance (R_s) serves a dual purpose: limiting the peak discharge current of the capacitor through the transistor during turn-on and allowing its complete discharge during the active duty-cycle. The minimum resistive value is obtained using (4):

$$R_s \geq \frac{V_D}{I_M \cdot I_L} = \frac{170\ \text{V}}{20\ \text{A} - 5\ \text{A}} \geq 11.33\,\Omega \qquad (4)$$

In turn, the maximum resistance limit is restricted by the minimum turn-on time $T_{ON(min)}$. At a switching frequency of 10" kHz" (period of 100 µ"s") and assuming a minimum duty cycle of 1%, $T_{ON(min)}$ is equivalent to 1 µ"s" . Assuming a commercial snubber capacitance of 1" nF" , the upper limit is defined by (5):

$$R_s < \frac{T_{ON(min)}}{3 \cdot C_s} = \frac{1 \cdot 10^{-6}\ \text{s}}{3 \cdot 1 \cdot 10^{-9}\ \text{F}} < 333.3\,\Omega \qquad (5)$$

Based on the calculated envelope (11.33 Ω≤R_ s<333.3 Ω), commercial resistors from 47 Ω to 100 Ω were selected, since the residual power in the resistor per cycle, analytically evaluated, was 0.083" W" .

E. Signal Conditioning and DC Bus Measurement

For real-time monitoring and system protection, a signal conditioning circuit was implemented, allowing the microcontroller to read the physical voltage of the DC bus while logically isolating voltage peaks. A resistive voltage divider was designed to scale the high-voltage levels, (170" V" nominal and 220" V" under overvoltage conditions) to the logical operating range of the microcontroller analog-to-digital converter (ADC) which has a maximum reference of 3.3 V and a 12-bit resolution.

To standardize the design and withstand power dissipation, the upper branch (R_{top}) was built using a series arrangement of three 332" k" Ω axial resistors rated at 3/4" W" , while the lower branch (R_{bot}), connected to physical ground, was

set to 10 kΩ. The scaled voltage (V_{out}) entering the PA1 pin of the microcontroller is governed by (6):

$$V_{out} = V_{DC} \cdot \left(\frac{10\ k\Omega}{996\ k\Omega + 10\ k\Omega}\right) \quad (6)$$

This configuration provides a constant scaling ratio of 0.00994. The conversion to the continuous digital domain by the 12-bit ADC (whose values range from 0 to 4095) is analytically defined in Table II, establishing the logical thresholds for calibration, safe low-voltage operation, and the nominal tolerance limit.

Table II. Voltage behavior and adc mapping

Voltage (DC Bus)	***Scaled Voltage*** *(Vout)*	***Digital Value Read (ADC)***	***Operating Scenario***
0" V" (Off)	*0.000" V"*	*0*	*Zero calibration*
48" V" (Tests)	*0.477" V"*	*≈592*	*Low-voltage validation*
170" V" (Nominal)	*1.690" V"*	*≈2097*	*Nominal operation*
220" V" (Overvoltage)	*2.186" V"*	*≈2713*	*Safety limit*

III. Results

To safely validate the SPWM control logic, the phase shift between phases, and the behavior of the designed inverter bridge, a reduced-scale experimental test bench was implemented in the laboratory. The nominal bus was supplied by a regulated source stabilized at 48.87" V DC" and the inverter was operated in open loop coupled to a bank of resistive loads (incandescent lamps) configured in Star and Delta to evaluate the balance of the generated network. The physical assembly of this system, integrating the digital control stage and the power bridge, is illustrated in Fig. 3.

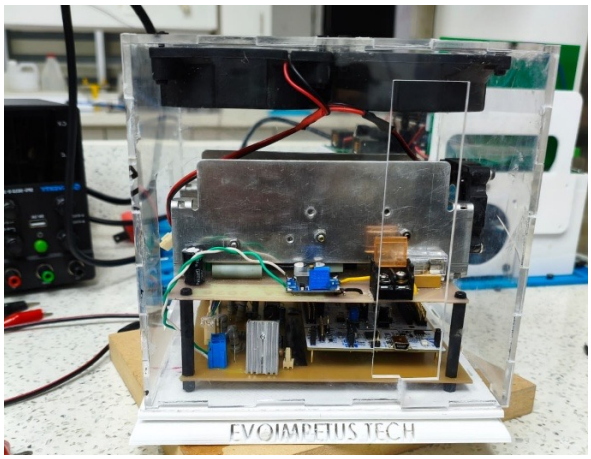


Fig. 3: *Physical prototype of the three-phase inverter*

A. SPWM Algorithm and Phase Shift Validation

The primary evaluation consisted of verifying the switching signals generated by the STM32 microcontroller before their injection into the power stage. Using an oscilloscope, it was confirmed that the developed algorithm successfully synthesized three sinusoidal envelopes with a phase shift of 120^ electrical degrees.

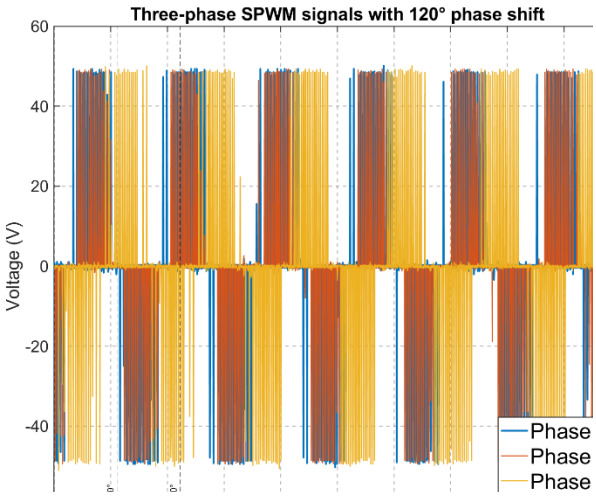


Fig. 4: *Experimental three-phase SPWM signals showing the (120^) electrical phase shift.*

In Fig. 4 shows the three SPWM phase signals recorded during the experimental validation. A vertical offset was applied only for visualization

purposes, allowing the phase relationship between the signals to be observed more clearly. The waveforms confirm the (120^) electrical phase shift between phases A, B, and C, validating the synchronization of the digital SPWM algorithm.

The fundamental output frequency remained stable (period of 16.66ms). In addition, the action of the dead-time safety band was visually verified, showing that the complementary signals did not overlap at any time. This confirmed the absence of signal overlaps and prevented the shoot-through phenomenon under the established test conditions. Under the Star (Y) load configuration, the differential voltage measured at the neutral point remained close to zero, and the line-to-line voltage waveforms were recorded at the output terminals, confirming the symmetry of the three-phase bridge.

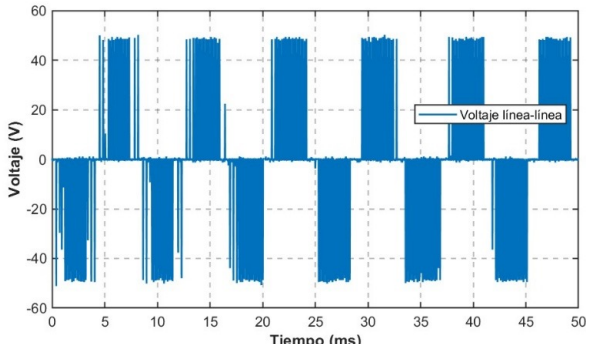


Fig. 5: *Line-to-line output voltage waveform V_AB, under SPWM modulation.*

As observed in Fig. 5, the measured signal corresponds to an unfiltered line-to-line PWM voltage. The envelope associated with SPWM modulation is identified from the variation in pulse width, while the final voltage waveform across the load depends on the harmonic content and the impedance seen by the inverter. The figure verifies the modulation logic and the phase shift between phases under the test conditions.

Although the total harmonic distortion (THD) was not experimentally measured in this stage, the selected switching frequency allows a preliminary theoretical estimation of the harmonic distribution. Considering a switching frequency of ($f_{s=3,kHz}$) and a fundamental output frequency of ($f_{o=60,Hz}$), the frequency modulation ratio is given by ($m_f=f_s/f_o=3000/60=50$). This indicates that the dominant harmonic components associated with the SPWM switching process are expected to be concentrated around the carrier frequency and its sidebands. Therefore, since the output voltage was measured without a filtering stage, future work should include experimental THD measurements and the design of an LC or LCL output filter to attenuate switching harmonics and improve the power quality of the inverter output, considering harmonic control criteria such as those established in IEEE 519-2022 [11].

B. Power and Energy Efficiency

Analysis

To evaluate the electrical and energy performance of the physical prototype, the input and output powers were measured during continuous operation with resistive loads. The power factor assumed for the incandescent lamps used in the test was unity.

In the direct current stage, the instrumentation recorded the bus voltage and the input current under steady-state conditions. Based on these data, the total input power consumed by the system was determined using (7):

$$P_{in} = 6.793\ \text{W} \qquad (7)$$

In the alternating current stage, the line-to-line voltages (V_{LL}) were measured across the resistive loads, and the current associated with the test was recorded. Using the average voltage value and the measured current, the three-phase active output power was calculated using (8):

$$P_{out} = 3 \cdot \sqrt{3} \cdot V_{LL} \cdot I_L \cdot cos(\phi) \qquad (8)$$
$$P_{out} = 6.3156W$$

Finally, the overall efficiency of the converter under these experimental conditions was estimated from the power ratio indicated in (9):

$$\eta = 92.97\% \qquad (9)$$

C. Discussion of Efficiency and Fixed Losses

The experimental efficiency obtained by the prototype was 92.97% under low-voltage and low-load laboratory conditions. This value should not be interpreted as the maximum rated efficiency of the inverter, since the system was evaluated in open-loop operation, with purely resistive loads, without an output filter, and operating below its rated power capacity.

The result obtained is consistent with otherstudies on low-power three-phase inverters. For instance, Lujara reported experimental efficiencies that did not fall below 92%, with values ranging approximately from 92.1% to 94.9%, depending on the load condition [12]. In comparison, more optimized topologies, such as multilevel or transformerless inverters, typically exhibit efficiencies exceeding 96% under different operating, power, and control conditions [1]. Therefore, the performance difference is primarily associated with the power level, the employed topology, the presence of filtering stages, and the control strategy. In this context, the 92.97% efficiency achieved during the tests confirms the adequate performance of the prototype under the evaluated experimental conditions, considering that the hardware-based dead-time insertion prevented cross-conduction between complementary signals and ensured the safe operation of the power stage. Nevertheless, elements such as the control board, gate drivers, cooling system, and the switching process represent inherent power consumptions and losses associated with the system's operation. For this reason, additional tests at higher load levels are required to determine the efficiency trend of the inverter under conditions closer to its rated operating point.

III. Conclusiones

The obtained results made it possible to verify the generation of three modulated signals with a 120° electrical phase shift, confirming the functionality of the developed firmware to produce a balanced three-phase system at low voltage. The dead-time insertion prevented overlap between complementary signals and protected the semiconductors during switching operations. The prototype operated stably during the tests with resistive loads in star and delta configurations. The measurements showed line voltages with close values and balanced behavior under the considered laboratory conditions. During the low-load tests, the prototype achieved an efficiency close to 92%. This result is influenced by the system's internal consumption when the transferred power is reduced. The energy characterization must be completed with tests at higher load levels and with an explicit definition of the voltage and current magnitudes used in the calculation. As future work, the inverter should be validated at higher load levels, total harmonic distortion (THD) measurements should be incorporated, its performance with inductive loads or three-phase motors should be evaluated, and filtering, interconnection, and power quality criteria should be analyzed if the prototype is oriented toward microgrid applications.

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